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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,828	09/11/2003	David R. Hembree	99-0812.2	5963

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EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,828	HEMBREE ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/6/03; 11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of "a plurality" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 47-67 are rejected under 35 U.S.C. 102(e) as being anticipated by Gilleo et al. (U.S. 6,204,455 B1).

Gilleo discloses a microelectronic element assembly with

(47) a semiconductor die (42) comprising a plurality die contacts (44) in a pattern;

a plurality of conductors (20) on the die (42) in electrical communication with the die contacts (44) configured redistribute the pattern of the die contacts (44);

a plurality of first contacts (44) on the die (42) in electrical communication with the conductors (20);

a plurality of second contacts on the die in electrical communication with the conductors (20) configured for electrical contact a test probe without electrical engagement of the first contacts (44) (see Figure 2);

(48) wherein the first contacts comprise bumps in an area array (see column 6, lines 35-38);

(49) further comprising an under bump metallization layer on each first contact (see Figure 2);

(50) wherein the second contacts comprise pads (see Figure 2);

(51) wherein the component is contained on a wafer (see column 12, line 3);

(52) further comprising an electrically insulating layer between the die and the conductors (see Figure 2);

(53) wherein conductors are configured to fan out or to fan in the pattern of the die contacts (see Figure 2);

(54) a semiconductor die having a face and a plurality of die contacts on the face in a pattern (see Figure 2);

a plurality of conductors on the face in electrical communication vith the die contacts configured redistribute the pattern of the die contacts (see Figure 2);

an electrically insulating layer on the conductors having a plurality of openings;

a plurality of first contacts on the face in electrical communication with the conductors (see Figure 2);

a plurality second contacts on the face in electrical communication with the conductors comprising pads aligned with the openings configured for electrical contact with a test probe (see column 2, lines 49-54. Figure 2);

(55) wherein the pads comprise portions of the conductors (see Figure 2);

(56) wherein the component comprises a semiconductor wafer;

(57) wherein the first contacts comprise balls in a ball grid array and each ball of the ball grid array is in electrical communication with a second contact (see Figure 2);

(58) a semiconductor wafer;

a plurality of components on the wafer comprising a plurality of die contacts;

a redistribution circuit on the wafer comprising a plurality of conductors in electrical communication with the die contacts;

a plurality test contacts on the wafer electrical communication with the conductors;

a plurality of terminal contacts on the wafer electrical communication with the conductors;

the test contacts configured for electrical contact by a test probe without interference from the terminal contacts, each test contact electrical communication with a terminal contact (see Figure 2);

(59) wherein the terminal contacts comprise under bump metallization layers and solder bumps (see Figure 2);

(60) further comprising an electrically insulating layer on the redistribution circuit having a plurality of openings aligned with the test contacts (see Figure 2);

(61) wherein the test contacts comprise portions of the conductors (see Figure 2);

(62) wherein the test probe comprises a needle probe, a buckle beam probe, a spring segment probe or a silicon probe;

(63) a semiconductor die comprising a plurality of die contacts in a pattern;

a plurality of redistribution conductors on the die in electrical communication with the die contacts (see Figure 2);

a plurality of bumped contacts on the die in electrical communication with the conductors;

a plurality of test contacts on the die electrical communication with the conductors, each test contact configured for electrical contact by a test probe without interference from the bumped contacts (see Figure 2);

(64) wherein the die is contained on a semiconductor wafer containing a plurality of dice substantially similar to the die (see Figure 2);

(65) wherein the bumped contacts comprise solder balls and under bump metallization layers in a grid array;

(66) wherein the test contacts comprise portions of the redistribution conductors (see Figure 2);

(67) wherein the test contacts comprise separate pads (see Figure 2).

Claims 47-67 are rejected under 35 U.S.C. 102(b) as being anticipated by Sumi et al. (U.S. 5,767,528).

Sumi discloses a semiconductor device with

(47) a semiconductor die (11) comprising a plurality die contacts (16) in a pattern;

a plurality of conductors (20) on the die (42) in electrical communication with the die contacts (16) configured redistribute the pattern of the die contacts (16);

a plurality of first contacts (16) on the die (11) in electrical communication with the conductors (20);

a plurality of second contacts (14) on the die (11) in electrical communication with the conductors (20) configured for electrical contact a test probe without electrical engagement of the first contacts (16) (see Figure 3);

(48) wherein the first contacts comprise bumps in an area array (see Figure 3);

(49) further comprising an under bump metallization layer on each first contact (see Figure 3);

(50) wherein the second contacts comprise pads (see Figure 3);

(51) wherein the component is contained on a wafer (see column 12, line 3);

(52) further comprising an electrically insulating layer between the die and the conductors (see Figure 3);

(53) wherein conductors are configured to fan out or to fan in the pattern of the die contacts (see Figure 3);

(54) a semiconductor die having a face and a plurality of die contacts on the face in a pattern (see Figure 3);

a plurality of conductors on the face in electrical communication with the die contacts configured redistribute the pattern of the die contacts (see Figure 3);

an electrically insulating layer on the conductors having a plurality of openings;

a plurality of first contacts on the face in electrical communication with the conductors (see Figure 3);

a plurality second contacts on the face in electrical communication with the conductors comprising pads aligned with the openings configured for electrical contact with a test probe (see column 9, lines 12-53. Figure 3);

(55) wherein the pads comprise portions of the conductors (see Figure 3);

(56) wherein the component comprises a semiconductor wafer (see column 9, lines 46-47);

(57) wherein the first contacts comprise balls in a ball grid array and each ball of the ball grid array is in electrical communication with a second contact (see Figure 3);

(58) a semiconductor wafer;

a plurality of components on the wafer comprising a plurality of die contacts;

a redistribution circuit on the wafer comprising a plurality of conductors in electrical communication with the die contacts;

a plurality test contacts on the wafer electrical communication with the conductors;

a plurality of terminal contacts on the wafer electrical communication with the conductors;

the test contacts configured for electrical contact by a test probe without interference from the terminal contacts, each test contact electrical communication with a terminal contact (see column 9, lines 12-53. Figure 3);

(59) wherein the terminal contacts comprise under bump metallization layers and solder bumps (see Figure 3);

(60) further comprising an electrically insulating layer on the redistribution circuit having a plurality of openings aligned with the test contacts (see Figure 3);

(61) wherein the test contacts comprise portions of the conductors (see Figure 3);

(62) wherein the test probe comprises a needle probe (see column 5, lines 24-28);

(63) a semiconductor die comprising a plurality of die contacts in a pattern;

a plurality of redistribution conductors on the die in electrical communication with the die contacts (see Figure 3);

a plurality of bumped contacts on the die in electrical communication with the conductors;

a plurality of test contacts on the die electrical communication with the conductors, each test contact configured for electrical contact by a test probe without interference from the bumped contacts (see column 9, lines 12-53. Figure 3);

(64) wherein the die is contained on a semiconductor wafer containing a plurality of dice substantially similar to the die (see Figure 3);

(65) wherein the bumped contacts comprise solder balls and under bump metallization layers in a grid array (see Figure 3);

(66) wherein the test contacts comprise portions of the redistribution conductors (see Figure 3);

(67) wherein the test contacts comprise separate pads (see Figure 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 3, 2004

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